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FIG. 1   PRIOR ART

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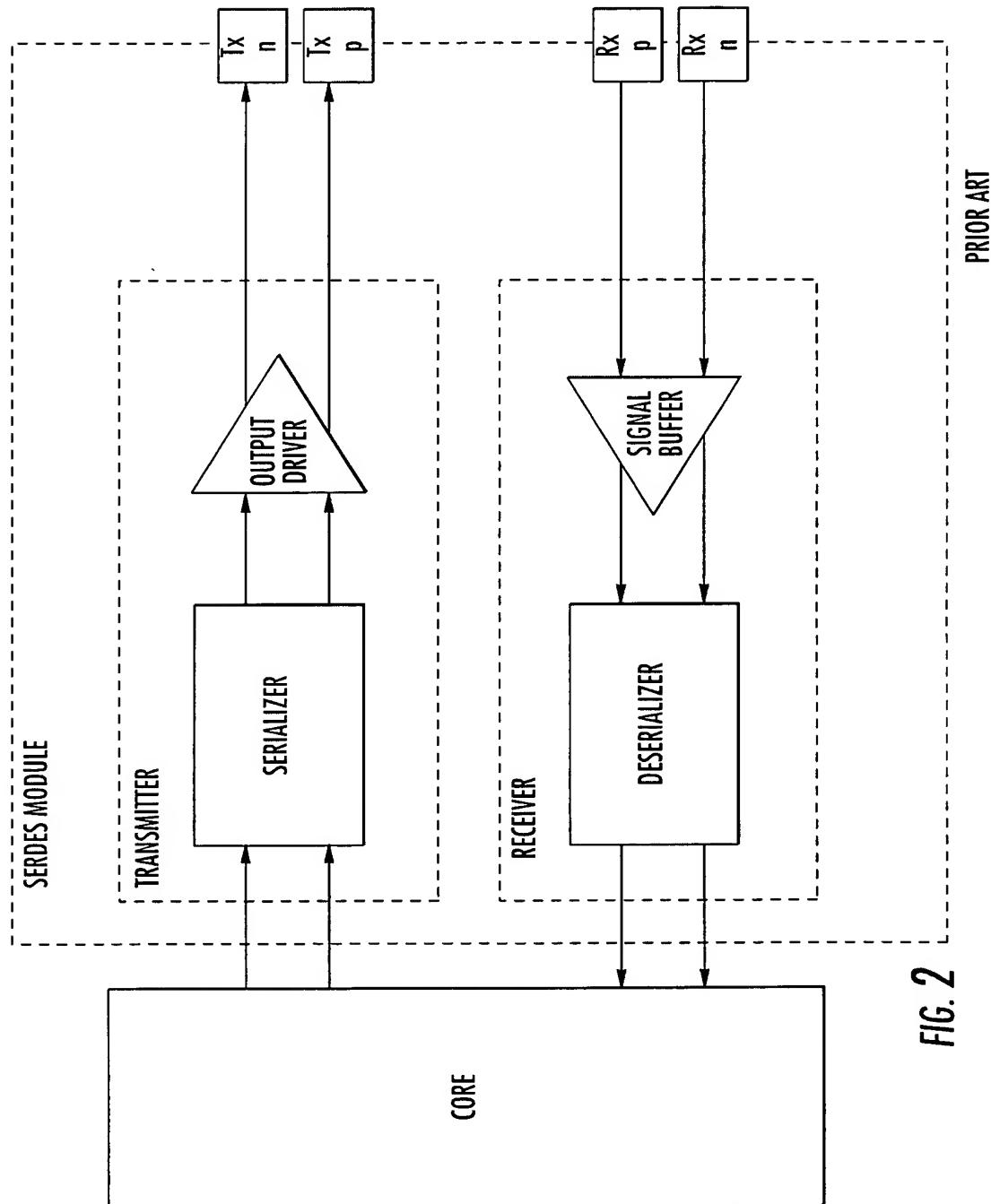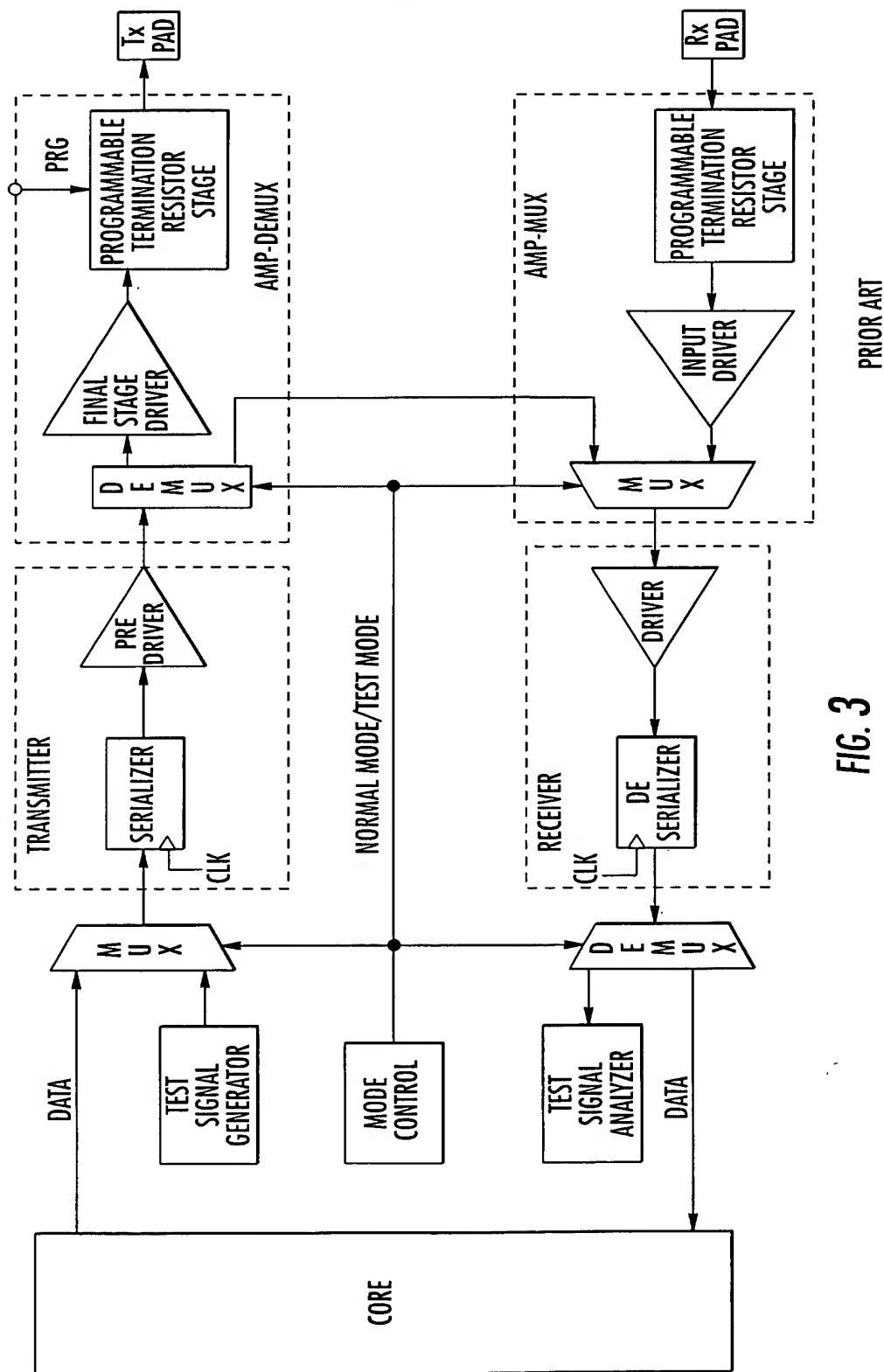
PRIOR ART

FIG. 2

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FIG. 3

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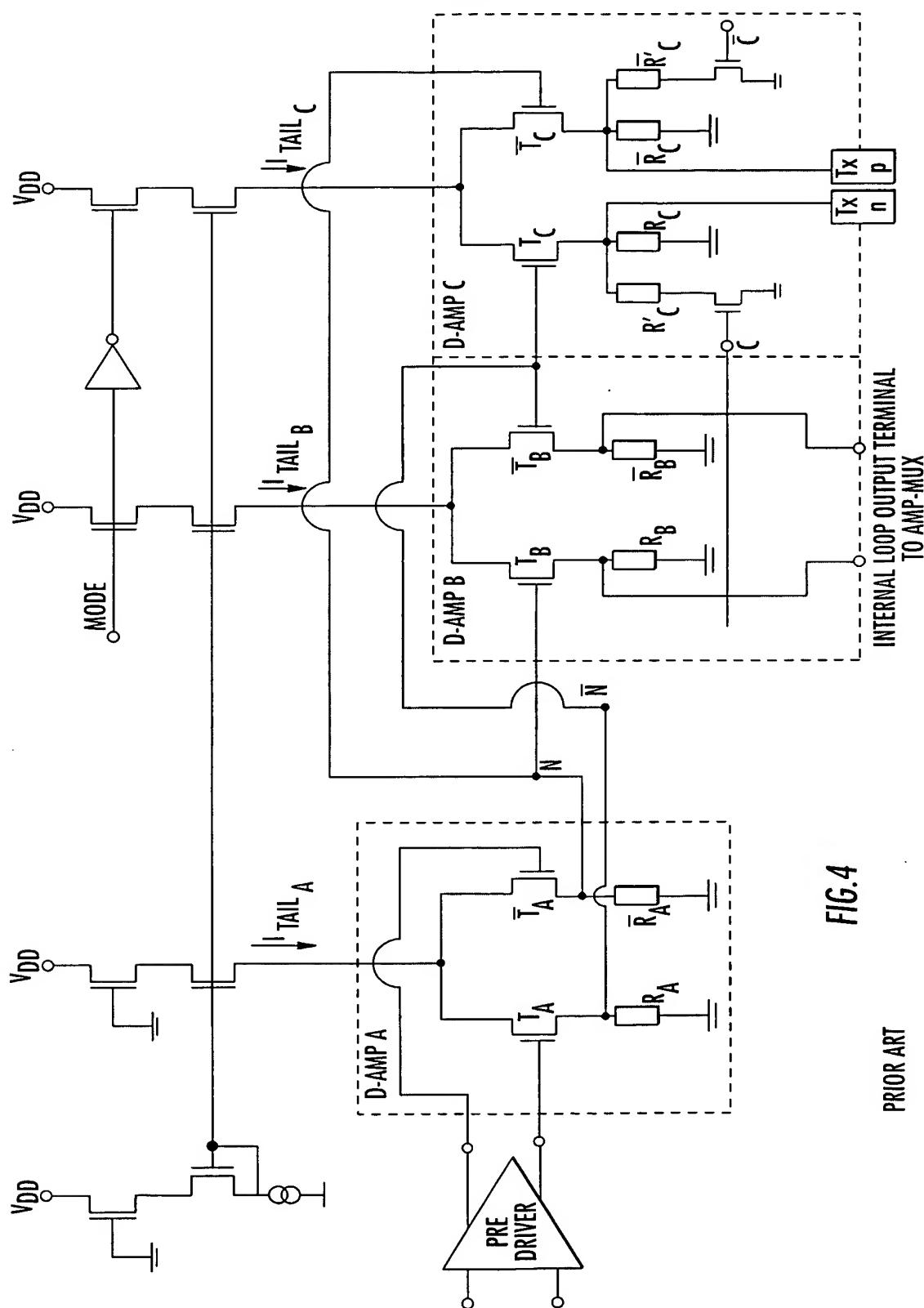
FIG.4

PRIOR ART

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FIG. 5

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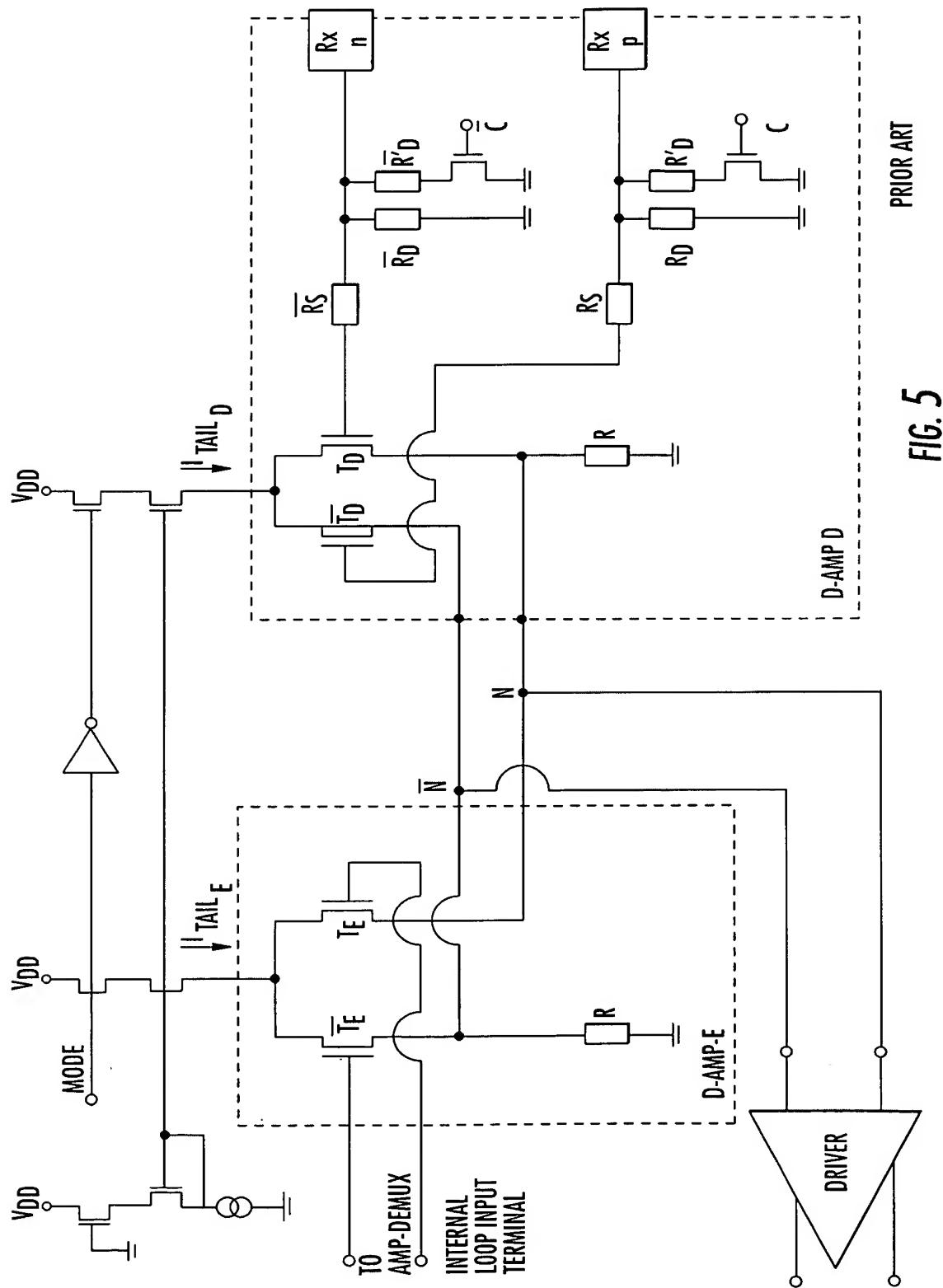
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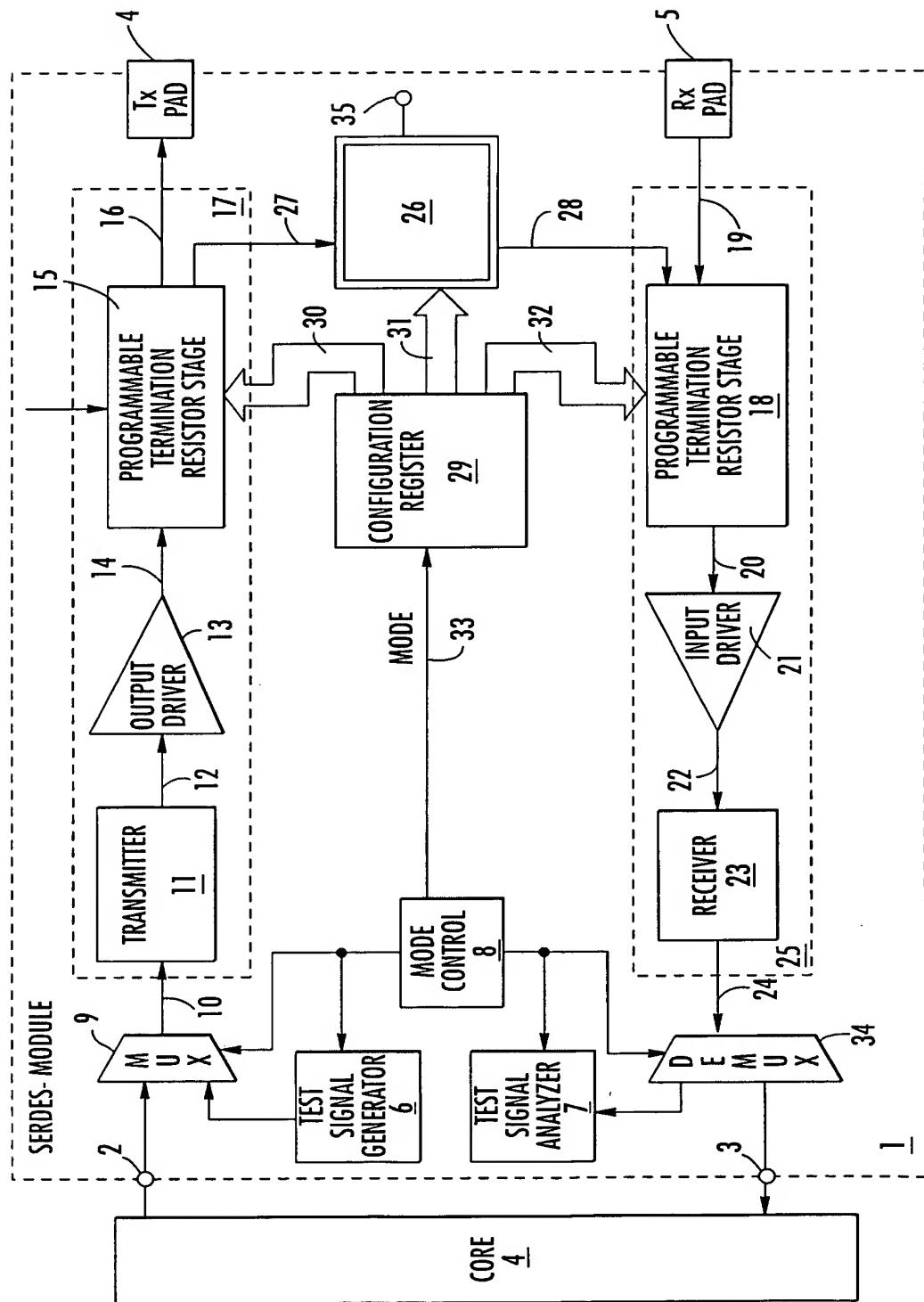
FIG. 6

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FIG. 7
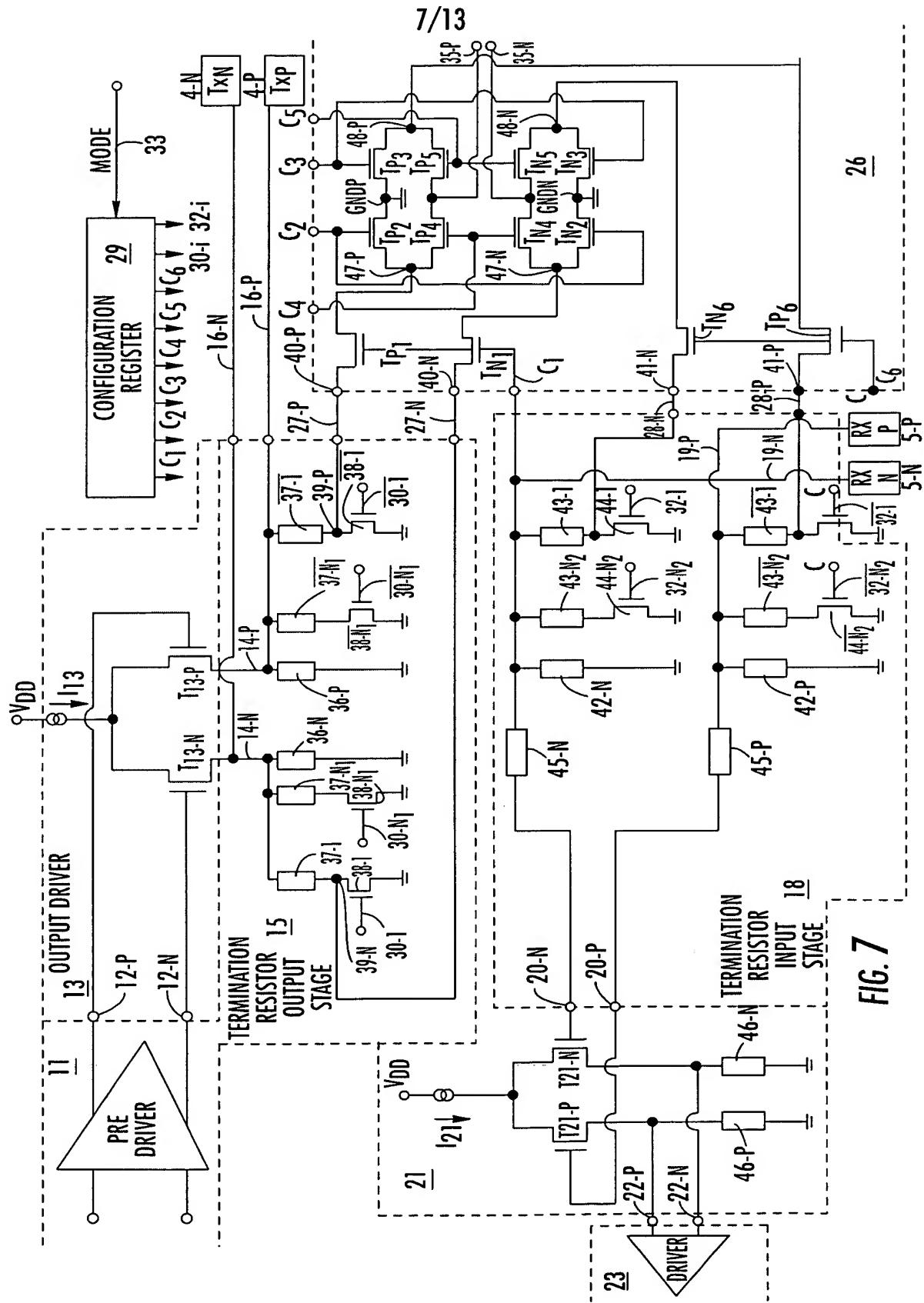
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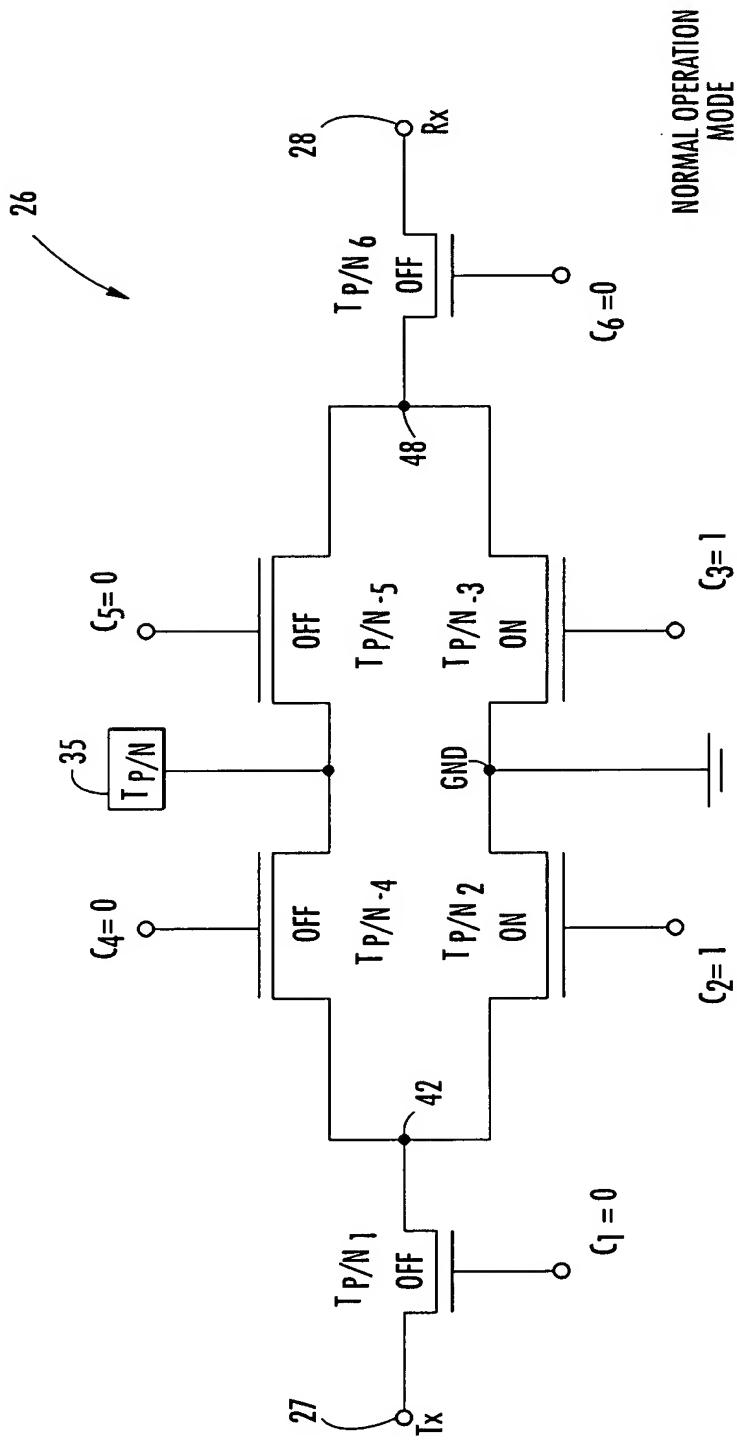
FIG. 8

NORMAL OPERATION MODE

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FEEDBACK
LOOP TEST MODE

FIG. 9

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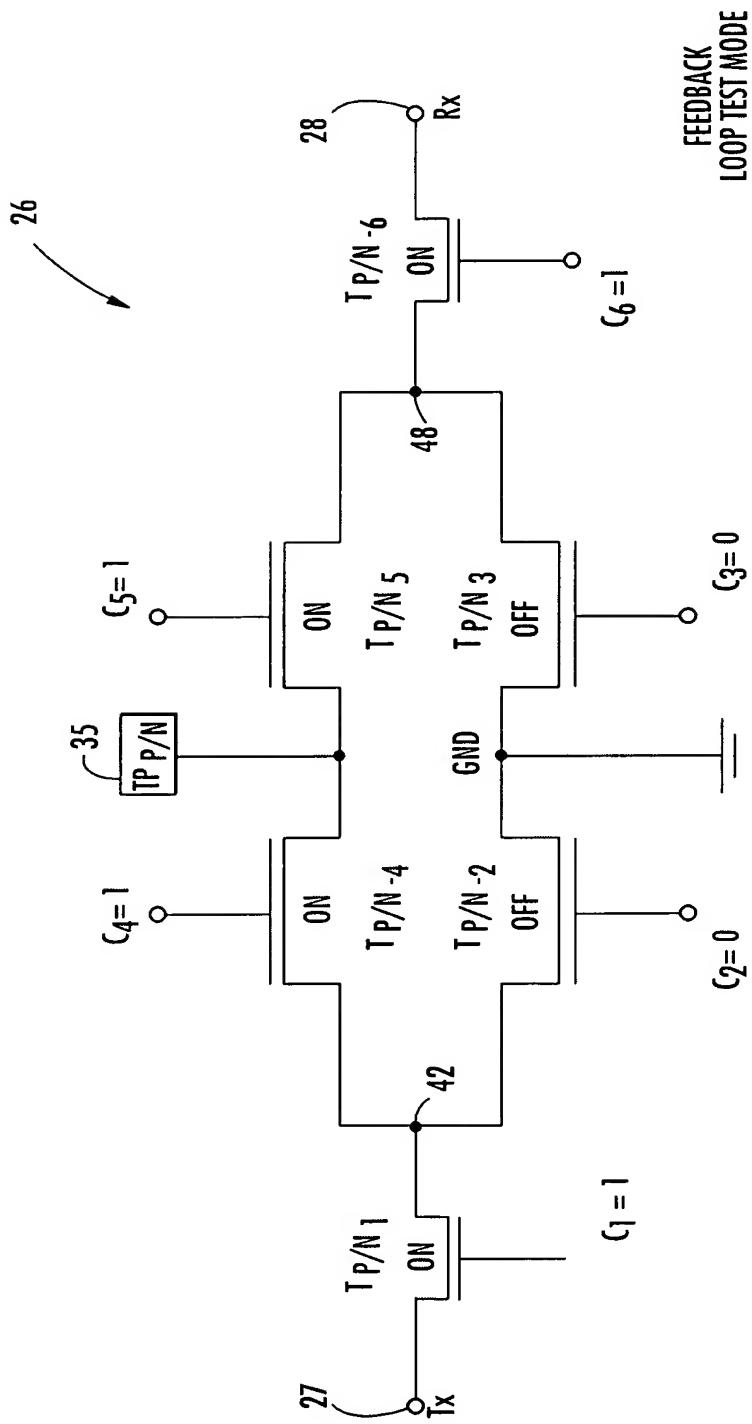
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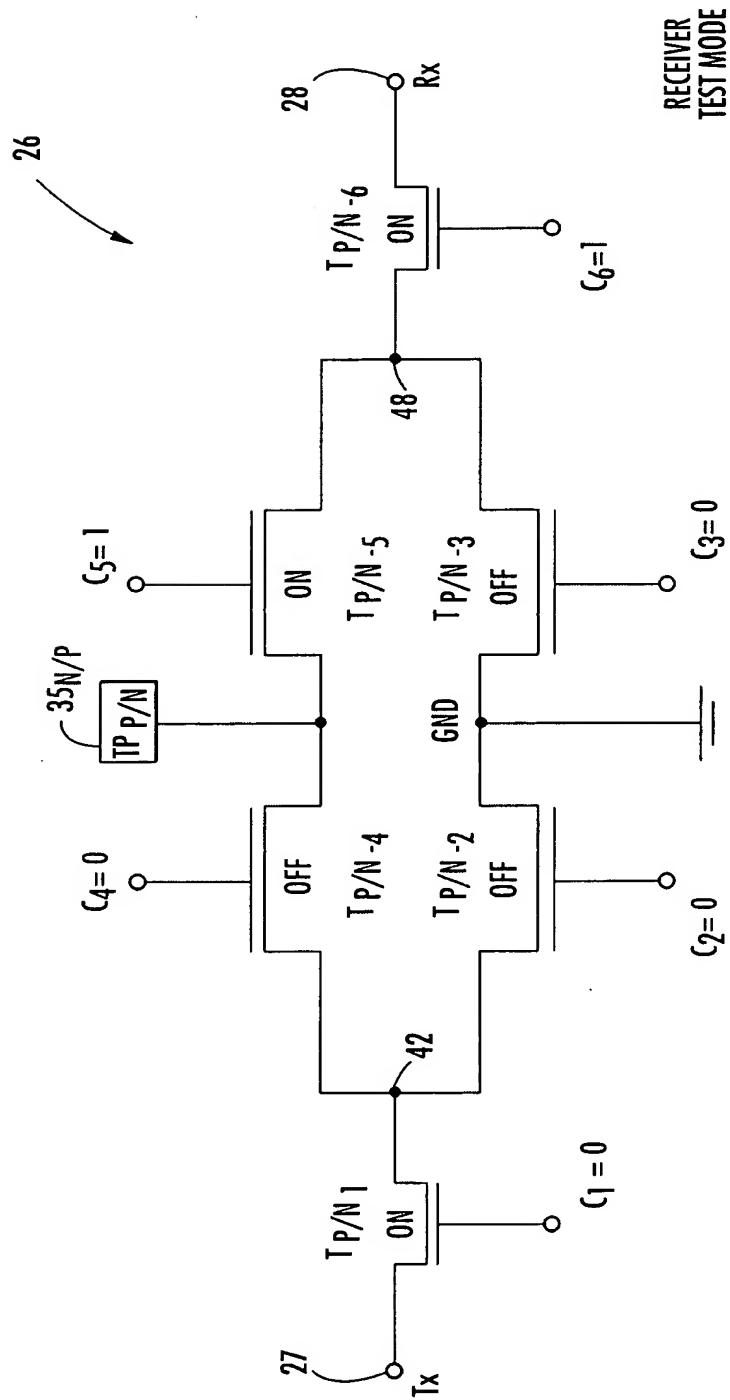
FIG. 10

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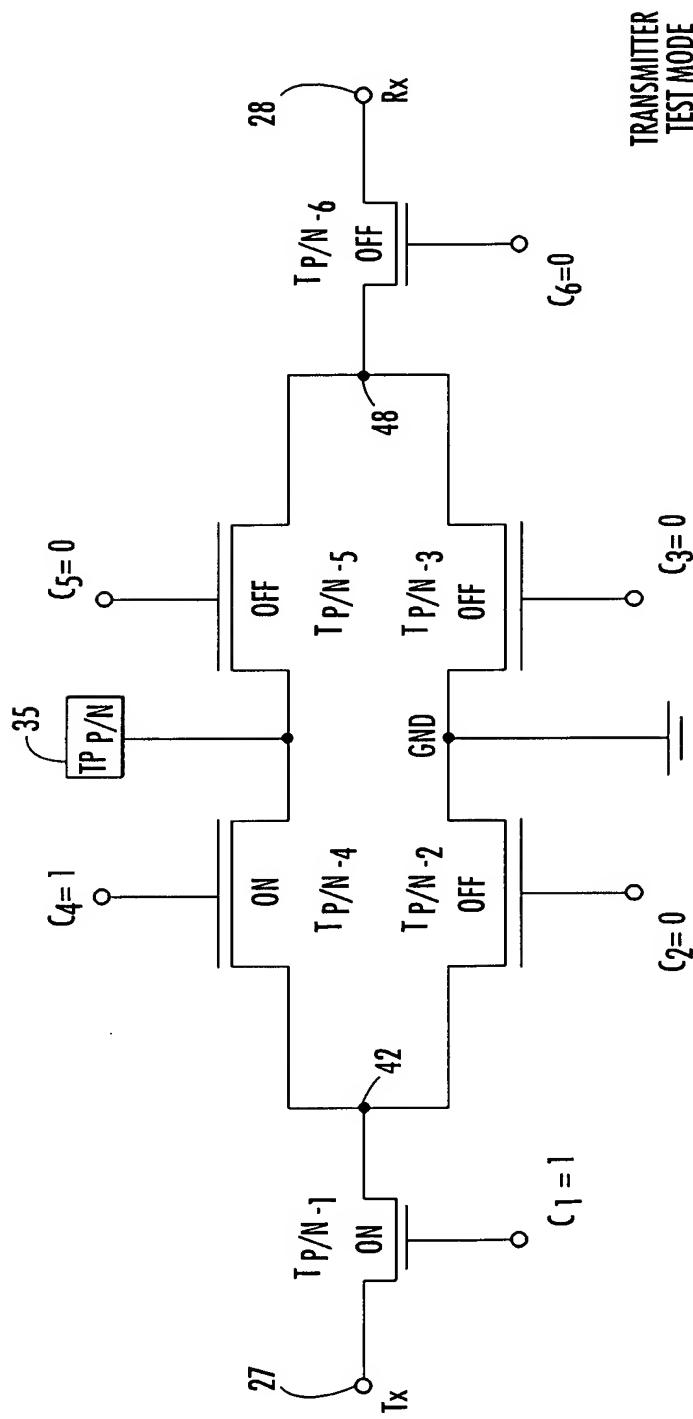
FIG. 17

TRANSMITTER TEST MODE

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CONFIGURATION REGISTER

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|	
C_{N1}^{Tx}	
C_{N2}^{Tx}	
$\vdots$	**CONFIGURATION OF PROGRAMMABLE RESISTORS ON TRANSMITTING (Tx) SIDE**
C_{NM}^{Tx}	
C_{P1}^{Tx}	
C_{P2}^{Tx}	
$\vdots$	
$C_{PM'}^{Tx}$	
C_{N1}^{Rx}	
C_{N2}^{Rx}	
$\vdots$	**CONFIGURATION OF PROGRAMMABLE RESISTORS ON RECEIVING (Rx) SIDE**
C_{NM}^{Rx}	
C_{P1}^{Rx}	
C_{P2}^{Rx}	
$\vdots$	
$C_{PM'}^{Rx}$	
C_1	
C_2	
C_3	**MODE CONTROL BITS**
C_4	
C_5	
C_6	
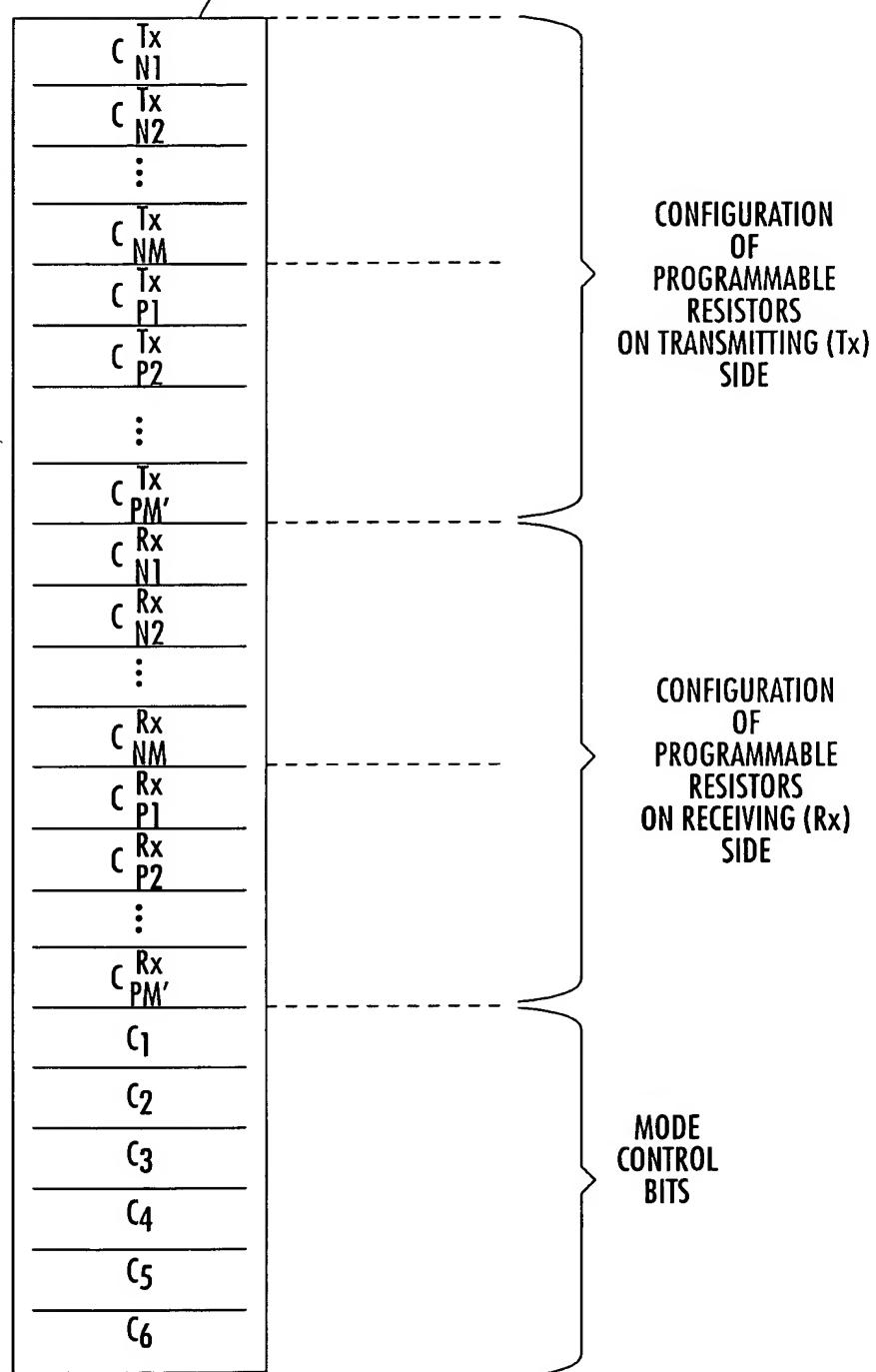
FIG. 12

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CONTROL BITS	NORMAL OPERATION MODE	FEEDBACK TEST MODE	RECEIVER TEST MODE	TRANSMITTER TEST MODE
C_1	0	1	0	1
C_2	1	0	0	0
C_3	1	0	0	0
C_4	0	1	0	1
C_5	0	1	1	0
C_6	0	1	1	0

FIG. 13